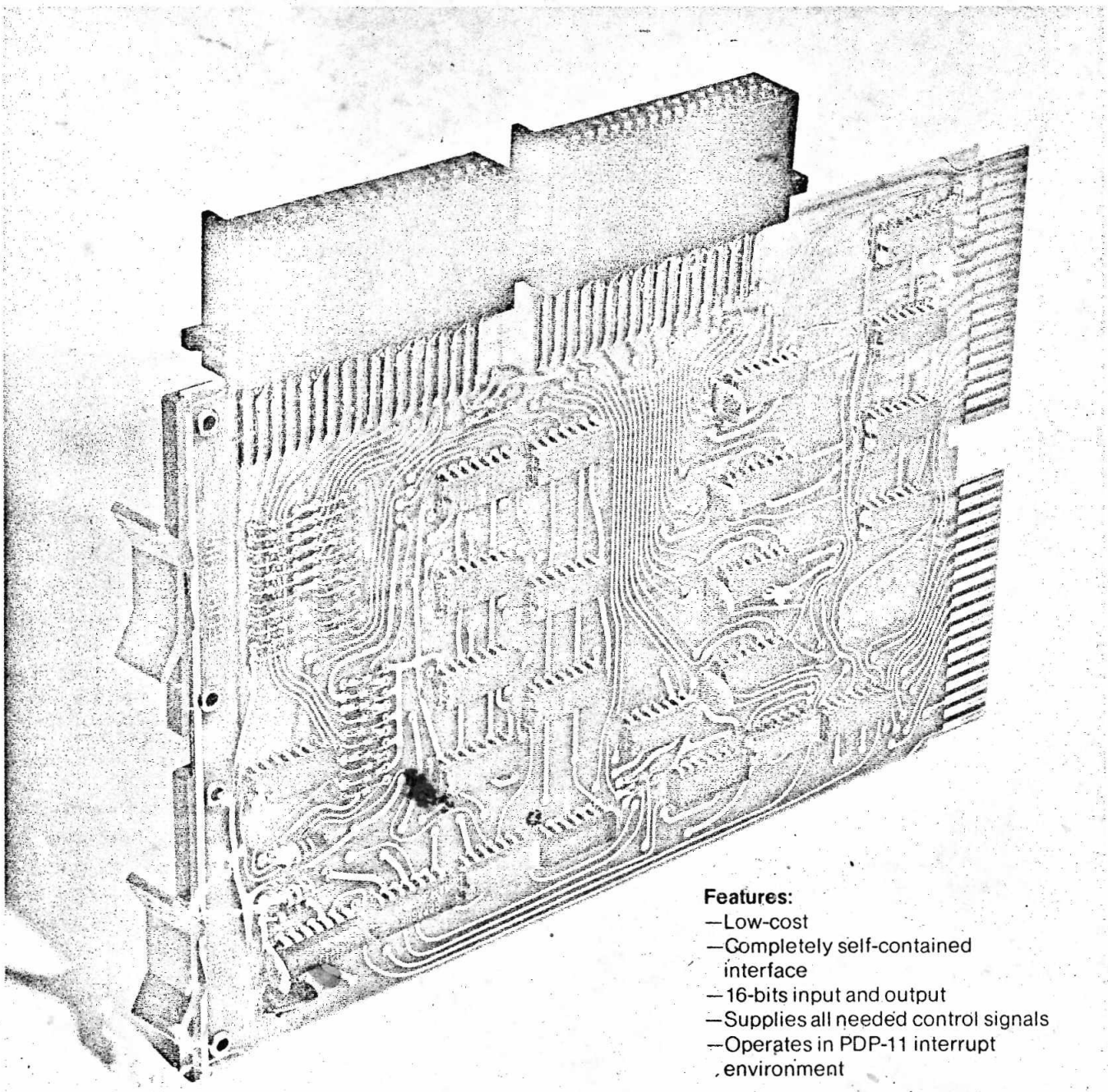
DIGITAL EQUIPMENT CORPORATION

pdp-11

OPTION BULLETIN

PDP-11 DEVICE REGISTER INTERFACE DR11-A



Features:

—Low-cost
—Completely self-contained interface
—16-bits input and output
—Supplies all needed control signals
—Operates in PDP-11 interrupt environment

digital

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The DR11-A Device Register Interface is a set of three logic modules which form a self-contained interface between the PDP-11 UNIBUS and a user's peripheral. The DR11-A performs all of the necessary tasks to communicate with the PDP-11, so that the user may easily interface his device. The simplicity and low cost of the DR11-A demonstrates the utility and power of the PDP-11 UNIBUS concept.

The DR11-A permits bidirectional transfer of 16-bits of information between a user's device and PDP-11 UNIBUS . The three functional sections of the DR11-A are: the M786 16-bit I/O Buffer, the M782 Bus and Interrupt Control Unit, and the M105 Address Selector Unit.

OUTPUT—Information from the UNIBUS is stored in a 16-bit buffer register. Once this register has been set under program control, the outputs are available to the device until the register is loaded with new data from the UNIBUS. The register can also be read onto the UNIBUS.

INPUT—The DR11-A also provides 16 lines of input to UNIBUS transmitters. This allows data from user devices to be read onto the UNIBUS. These signals are not held in the flip-flop register of the DR11-A.

CONTROL—Upon data transfer to the buffer register, a control signal, NEW DATA READY, indicates to the device that data has been loaded into the register. For input onto the UNIBUS, a control signal, DATA TRANSMITTED, indicates to the device that the input lines have been read.

Two interrupt request lines provide the ability to make vectored interrupt requests to the PDP-11 processor through two sets of unique vector addresses. Interrupt enable/disable circuits are controlled by bits 6 and 5 of the addressable DR11-A control register.

Complete information for designing with the DR11-A is supplied in the PDP-11 UNIBUS Interface Manual, available upon request.

Register Addresses

Control	177520	Standard factory setting.
Buffer	177522	May be changed by jumpers on M105
Input	177524	
Vector Address A	110	Standard factory setting.
Vector Address B	114	May be changed by jumpers on M782.

Priority Level

5 normal — May be changed by priority jumper plug on M786.

Input Levels

+3V = 1, 0V = 0
1 TTL unit load

Output Levels

+3V = 1, 0V = 0
capable of driving 8 TTL loads

Signal Connections

Input, output, control and ground signals are available on two H807 connectors mounted on the M786. Connections are normally made to the H807's via M925 (flexprint connector card) or M927 (cable connector cards with solder lugs for ribbon cable or twisted pairs). Two M927 Connector Cards are supplied.

Environmental

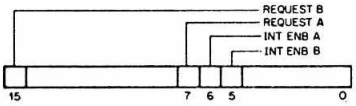
Temperature	10° —50° C
Humidity	20%—90% non condensating

Physical

Mounts in one small peripheral slot in KA11 or DD11-A.
Power derived from H-720 in BA11.

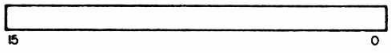
Registers

Control Register



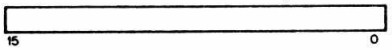
INT ENB A	Enables Interrupt requests from request line A.
INT ENB B	Enables Interrupt requests from request line B.
	Both may be set or cleared from Unibus. Both are cleared by START or RESET.
REQUEST A	Indicates status of REQUEST A line; +3V=1, 0V=0.
REQUEST B	Indicates status of REQUEST B line; +3V=1, 0V=0.

Buffer Register

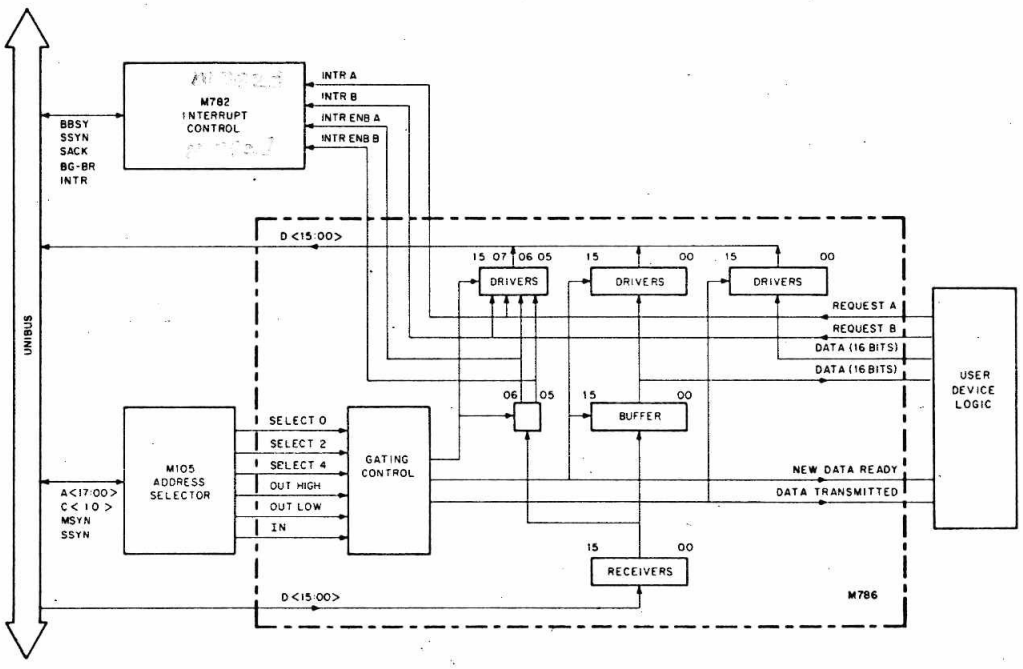


All bits may be cleared or set from Unibus. Register cleared by START or RESET. Outputs available to user.

Input Register

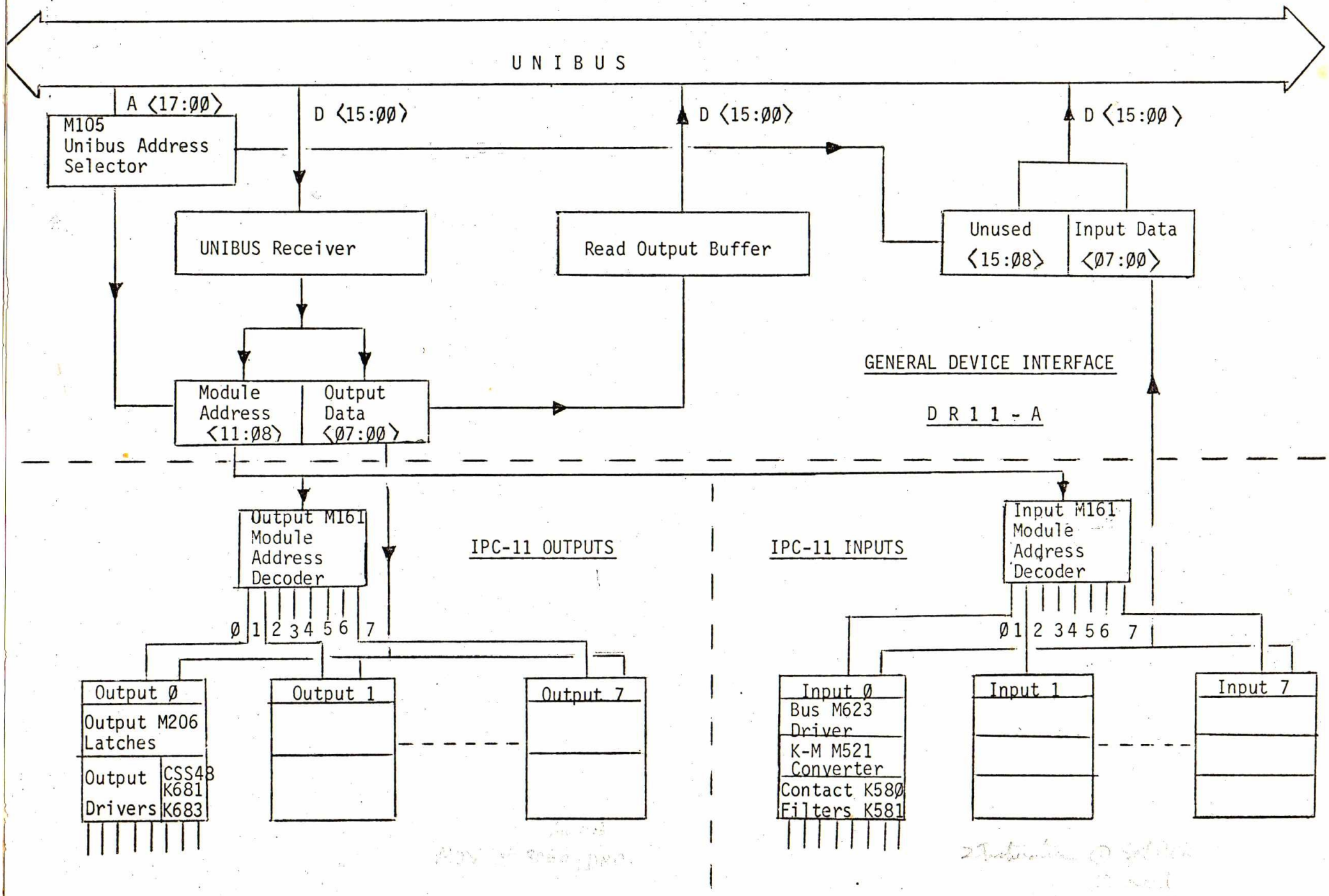


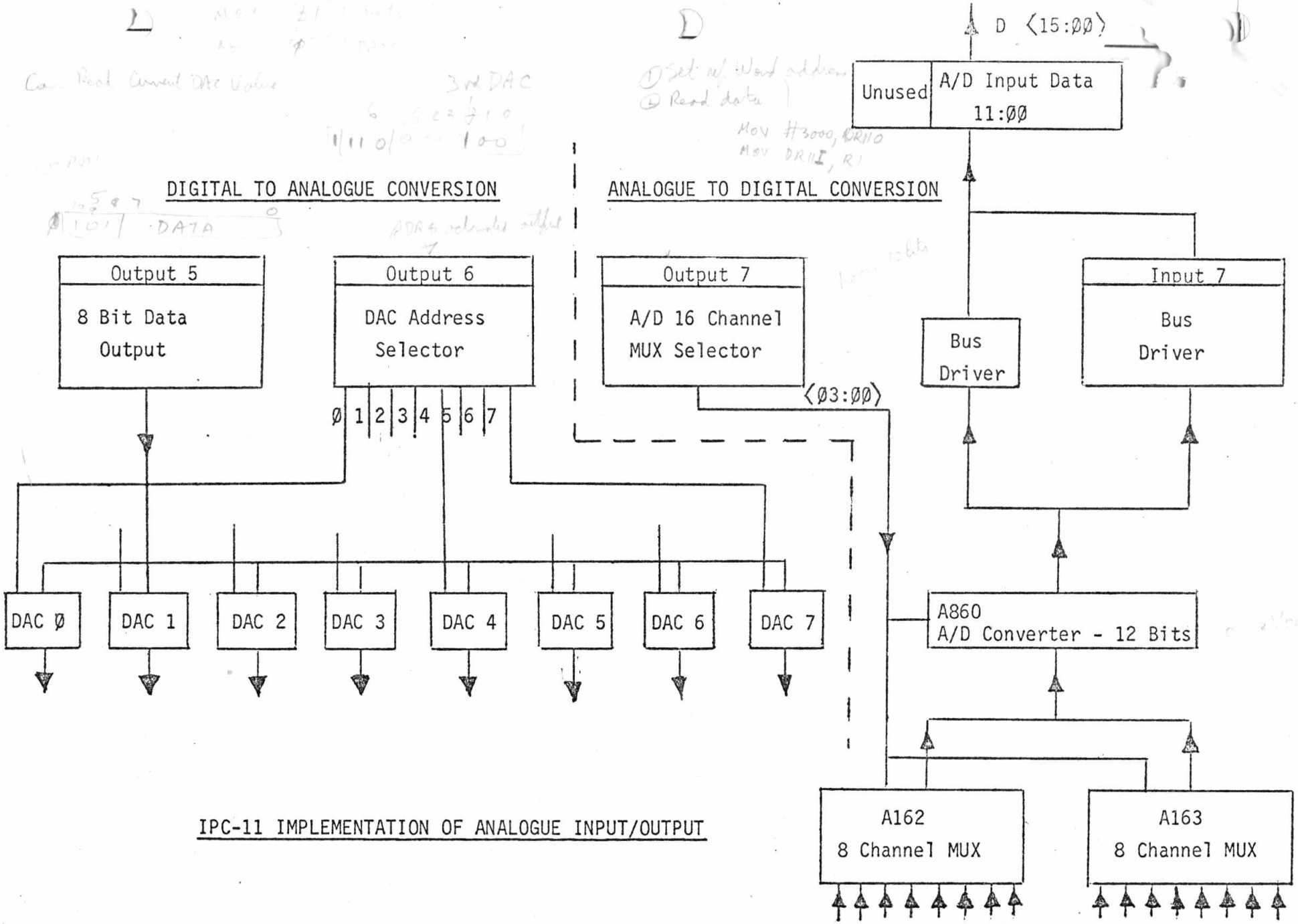
All bits may be read from UNIBUS. Bit status determined by user input lines.



DR11-A General Device Interface (block diagram)

IPC-11 SCHEMATIC BLOCK DIAGRAM





IPC-11 IMPLEMENTATION OF ANALOGUE INPUT/OUTPUT